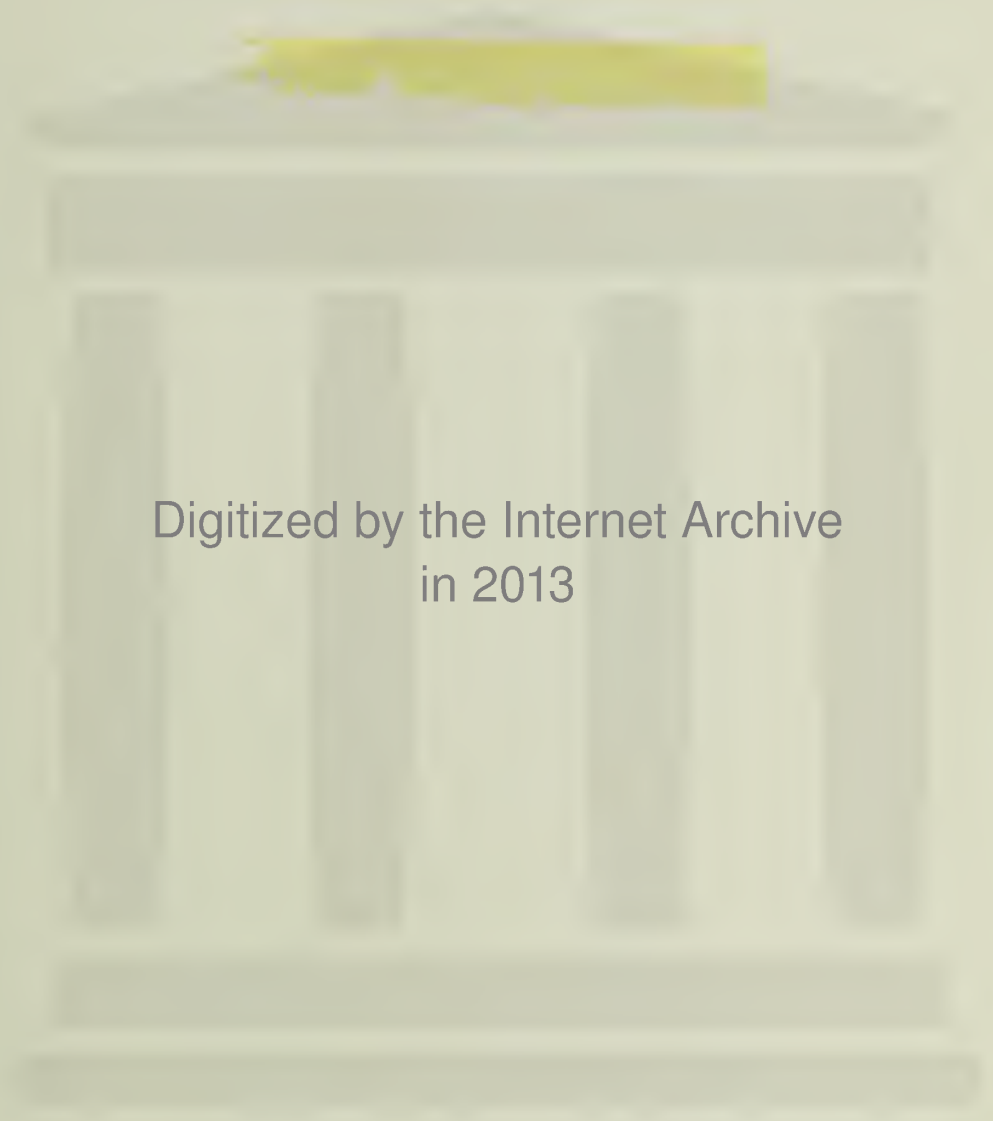

Report No. 220

COO-1469-0049

HYBRID CIRCUIT DESIGN OF THE ARTRIX GRAPHICAL PROCESSOR.

by

PETER ERNST RUDOLF OBERBECK

January 7, 1967

DEPARTMENT OF COMPUTER SCIENCE · UNIVERSITY OF ILLINOIS · URBANA, ILLINOIS

Report No. 220

HYBRID CIRCUIT DESIGN FOR THE ARTRIX GRAPHICAL PROCESSOR

by

PETER ERNST RUDOLF OBERBECK

January 7, 1967

Department of Computer Science
University of Illinois
Urbana, Illinois 61801

ACKNOWLEDGEMENT

The author wishes to express his gratitude to Professor W. J. Poppelbaum who conceived the basic Artrix System, and whose efforts made the actual construction possible. His enthusiasm even during difficult times was greatly appreciated by all.

Special thanks is also given to William Kubitz and David Rollenhagen for their design of the display and memory system, and to John Esch for his design of the digital processor. Furthermore, the author wishes to thank Al Irwin for his efforts in building the main frame and his help in debugging the system.

TABLE OF CONTENTS

LIST OF FIGURES

1. INTRODUCTION

As computer systems have become bigger and bigger it has become increasingly difficult for people to communicate with the computer effectively. Ideally one would just like to talk to a machine, and tell it about ones problem, and then have a reply come back in the form of a printed output, or a picture on a graphic display, or a spoken answer.

The printed form of question and reply is the most commonly used today. Some systems are capable of giving a spoken reply, but are not capable of receiving a spoken command. Graphical input and output have become a reality over the last few years and have shown great promise as being an efficient way of communicating with a computer.

Most graphical consoles used to date will generate or recognize a drawing or symbol on a point by point basis. Elaborate calculations and logic must be performed with each point in order to determine what to do with it. This type of processing obviously requires a great deal of computational equipment to process even the most trivial drawings, e.g., a straight line.

It seems, therefore, that the price one pays in "talking" to a computer through a graphical terminal is to use another computer as an interpreter. It seems to be a waste of expensive equipment to tie up a big machine with possibly trivial problems, and one begins to look for simple means to do graphical processing.

The Artrix Graphical Processor is a high speed, on-line graphical processor capable of doing all Euclidian constructions (those constructions that can be done through the use of a compass and straight-edge only) without the use of a large digital computer. It was conceived with the

idea in mind that graphical processing could be done rapidly and effectively through the use of both analog and digital circuitry. For graphical displays an accuracy of .3 percent is sufficient, hence simple digital and analog circuitry could be used. By making effective use of the best features of analog and digital circuits a minimum of total equipment was used, and high-speed graphical processing without the use of a large digital computer became reality.

In order to make use of both digital and analog circuitry one has to overcome the interface between the two. The design of hybrid digital-analog circuitry enables one to make the best use of each and becomes therefore a very important part of the design considerations of the Artrix system. Of particular interest is the DCVGLA (Digitally Controlled Variable Gain Linear Amplifier) whose function is to control the amplitude of a sinusoid in response to a digital input. The device is capable of digitally changing the amplitude over the range of 512 points at a speed of about 2 MHz. Response of the entire system is such that all drawings appear flicker-free and instantaneous as far as the operator is concerned. The effective use, need, and design of this and other practical hybrid circuits as regards graphical processing will be discussed in this thesis.

2. CAPABILITIES AND OPERATION OF THE SYSTEM

2.1 Line Construction

The operator is capable of constructing a line between any two points on the screen. First the construction points used are indicated with a light pen and appear on the display screen as dots. The operator now presses a button to put him in the line construction mode. Now, by pointing the light-pen in the neighborhood of a point and pressing an "enable" button on the pen he will store the coordinates of this point as point one. Similarly a second point is indicated. As soon as both points have been indicated an "execute construct" button will light up, and upon depressing it, a straight line will appear between the two points indicated. The operator can now translate this line to any other point on the screen by resetting and reindicating point one. This feature enables the operator to draw a series of parallel lines on the screen.

In actual Euclidian constructions one has to "construct" a parallel line using a compass and doing several operations before such a line may be drawn. Since it is often desired to construct parallel lines it was felt that this feature is essential to the system, although it is not a primary Euclidian construction.

2.2 Circle Construction

As in the line construction the operator can indicate a series of construction points on the screen with a light pen. He then goes to the circle construction mode by pressing the appropriate button. The first point he now indicates will correspond

to the center of the circle. Indicating a second point on the screen will correspond to indicating a point on the circumference of the circle. Again as in the line construction the circle will be drawn when the "execute construct" button is depressed.

The operator can now translate the circle with the same radius to any point on the screen, by reindicating point one. Similarly the radius can be changed by reindicating point two. This will result in constructing a circle with a new radius and using the previously indicated point one as the center. These two basic circle operations correspond to the actual operations one can carry out with a compass.

For both line and circle operation the construction points used to indicate the position and size of the lines can be erased by pushing a button marked "erase point". (Note that no constructions can be made without these construction points). This is done to avoid confusion between the construction point and a construction line or circle segment.

2.3 Erasing

If one wants to erase part of a line or circle, one first goes into the erase mode. The part of the construction that is now to be erased is traced over by the operator with the light pen. The part to be erased will appear black on the screen until the "execute erase" button is depressed. At this time the black lines and the "underlying" lines to be erased will disappear.

2.4 Freehand Construction

Should one encounter a drawing where it is necessary to draw something other than a circle or a line, one can go to a "write display" mode where it is possible to do freehand sketching or writing. All one has to do is to keep the enable button on the light-pen depressed as long as one wants to write.

This feature is especially useful for filling in gaps, and for lettering.

3. BASIC SYSTEM LAYOUT

Figure #1 shows a basic block diagram of the Artrix System.

3.1 Display and Storage System

The basic method used to store and display constructions and construction points is to have a vidicon look at a storage tube, which is simultaneously scanned (in synchronism) with a standard television monitor, and to gate the storage tube on each time the scan on the monitor intersects the light-pen. The light-pen is a photosensitive device, that will produce a short pulse each time the beam on the monitor scans past it. The point that occurs on the storage surface is then displayed on the point indicated by the light-pen on the monitor. This point will remain displayed until the storage tube is erased. It is interesting to note, that the vidicon merely provides an optical feedback path necessary to view what was written on the storage tube. One could still write on the storage tube even though the vidicon were not turned on. All constructions are done and stored on one storage tube. All construction points are stored on another storage tube. They are called display and point memories respectively. This enables the distinction of construction points from actual constructions by the processor, and also allows complete erasure of all construction points without indicating each one of them beforehand. One can also do freehand construction in either one of these storage tubes.

Figure #2 illustrates the vidicon-TV monitor-storage tube combination.

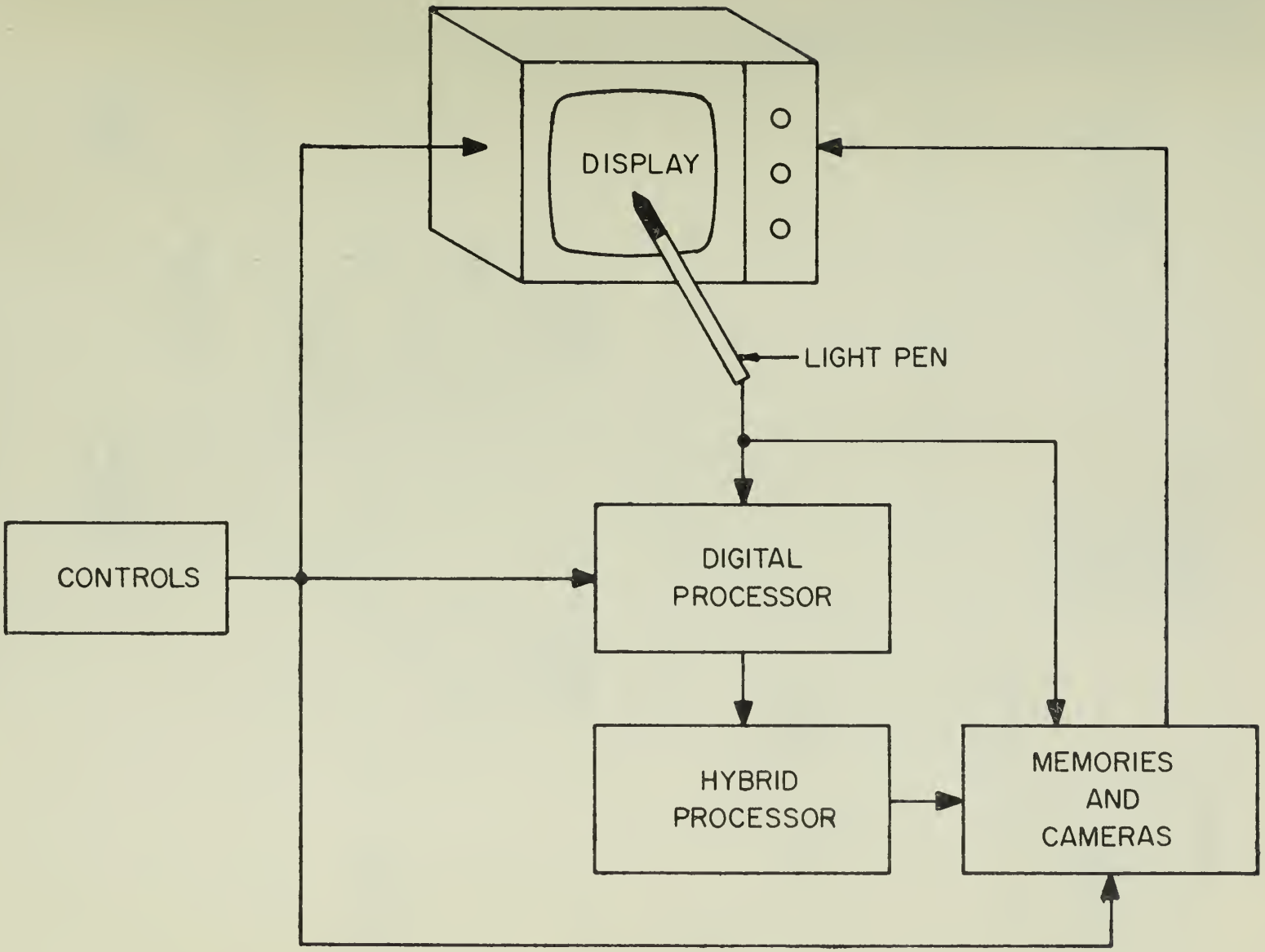

Figure #1. Block Diagram of System

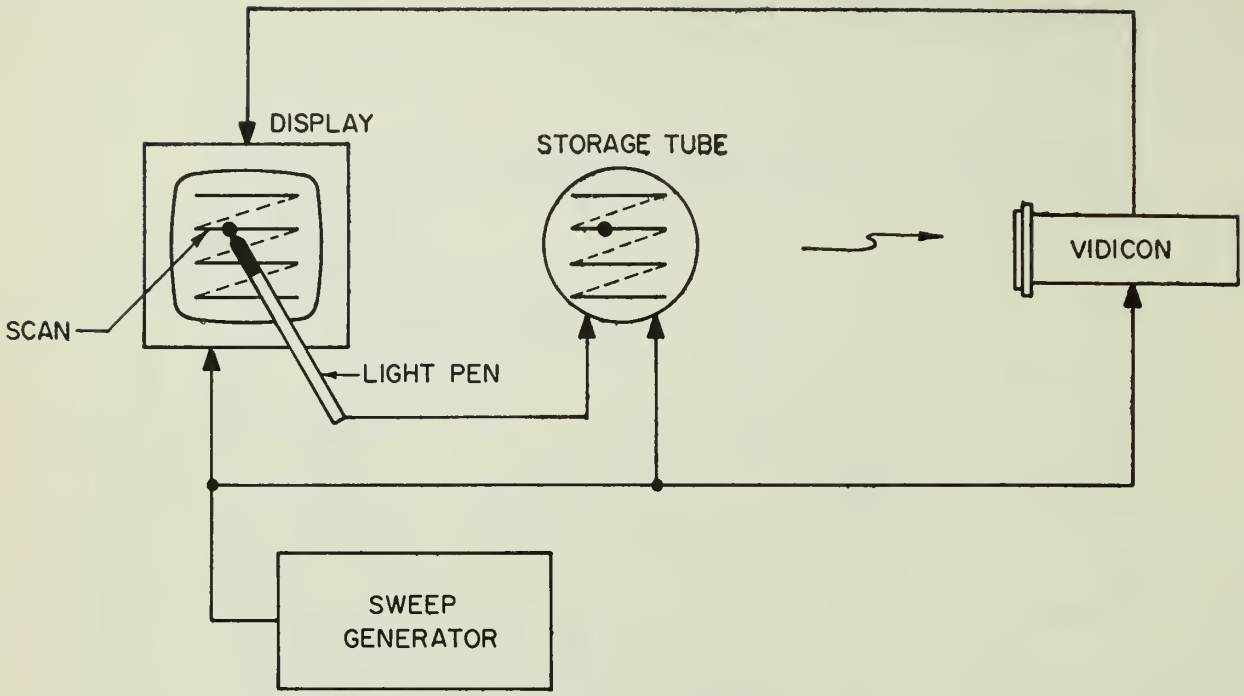

Figure #2. Storage-Display System.

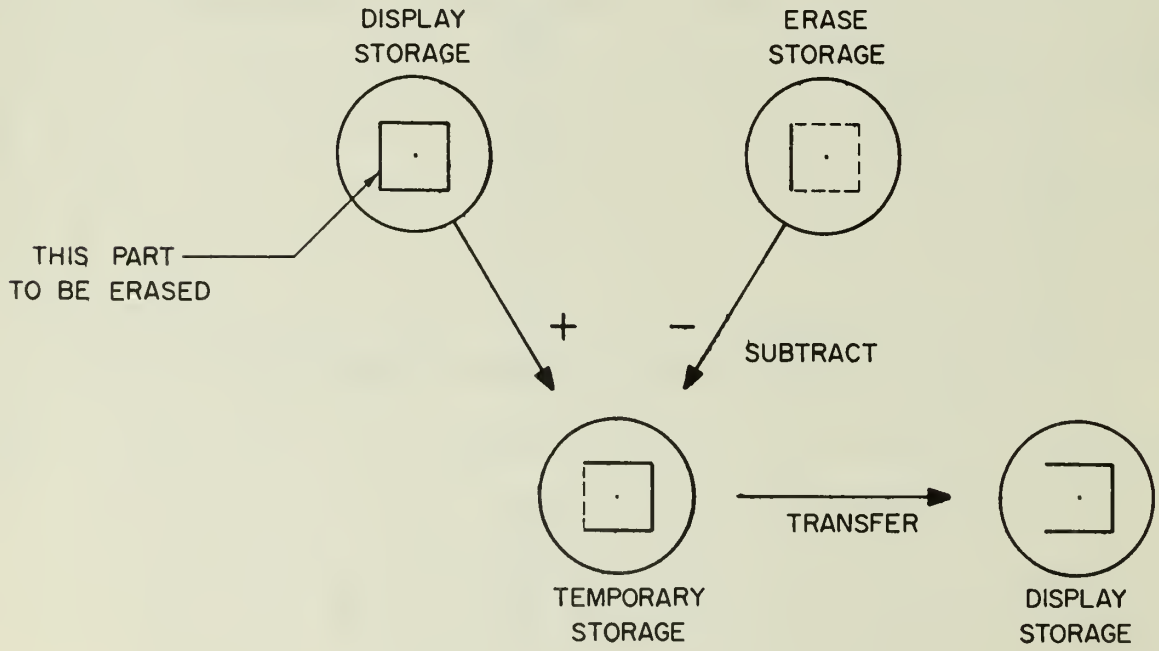

Figure #3. Erase Operation.

3.2 Local Erase System

In order to perform local erasure (which is not a feature of the storage tube) two more storage tubes are needed. One storage tube contains the information regarding the areas that should be erased (erase memory). The other temporarily stores the display information minus the points to be erased before it is transferred back to the display tube (Temp. memory). During erasing the following things take place. The parts of the drawing to be erased are traced over by the light pen, and are stored in the erase memory. Upon "erase execution" the negative of what is stored in the erase memory is now added with the display memory and the result is stored in the temporary memory. One can see that those parts stored in the erase memory and those that were also in the display memory have now cancelled each other out. As soon as the transfer to the temporary memory has taken place, the display memory is erased. Then the information in the temporary memory is transferred to the display memory. At the end the erase and temporary memory are erased. The result is that only these portions that were originally in the display memory and not traced over will reappear on the display memory. Figure #3 illustrates this operation.

4. GRAPHICAL PROCESSOR

The graphical processor of the Artrix system essentially consists of two main parts. One is the digital section, and the other is the hybrid digital-analog section. The operation of each of these sections may be subdivided into two more parts. One for the construction of lines, the other for the construction of circles.

The digital section essentially provides digital magnitudes for the size and translation of the analog signals. The hybrid circuitry uses these digital signals to provide actual analog signals corresponding to lines of proper size, slope and position as well as circles of proper size, and position. The actual analog signals are first sent to the display memory, from which they are shown on the display.

4.1 Generation of Circles

The storage tube employed in the Artrix System is essentially an oscilloscope with the property that any waveform displayed on it may be stored at the user's command. The problem then consists of supplying a waveform to the storage tube that will look like a circle. A sine and a cosine wave of equal amplitude and frequency applied to the vertical and horizontal deflection plates respectively will generate a circular pattern. Such a pattern is a very simple example of a Lissajous Pattern. Figures of a more complicated nature are usually encountered when displaying combinations of sinusoidal waveforms of different phase and frequency relationships. Using the two functions $R \sin(\omega t)$ and $R \cos(\omega t)$ a circle of radius R will be generated. If R is made variable, circles

of any size may be generated. If one wants to translate the circle in the vertical and horizontal directions, one merely adds a DC component to the R sin(ωt) and R cos(ωt) functions. We therefore concentrate on functions of the form:

$$V = R \sin(\omega t) + VP_1$$

$$H = R \cos(\omega t) + HP_1$$

which generate a circle of radius R translated vertically VP_1 units and horizontally HP_1 units from some zero reference. The actual generation of such a pattern is graphically illustrated in Figure #4. We now have a mechanism by which we can generate a circle of any radius and any translation, provided we can accurately control the values of R, VP_1, and HP_1. It will be shown later how digital values of R, VP_1, and HP_1 are generated and used to control the amplitudes of the sinusoidal functions and their respective DC offset component.

4.2 Generation of Lines

The generation of a line at first sight is even more trivial than that of a circle. This seems so because one only has to use the function R sin(ωt) or R cos(ωt). In fact, any two sinusoidal functions that are in phase will generate a straight line. The function R sin(ωt) applied to both horizontal and vertical plates of an oscilloscope will generate a line of length 2R sloping at $+45^{\circ}$ to the right. One can now see the difficulties involved in constructing a line between two points. If the slope should be variable (as is desired in this system) one must be able to control the magnitude as well as the sign of each sinusoid independently. For instance, lines with negative slope must have a

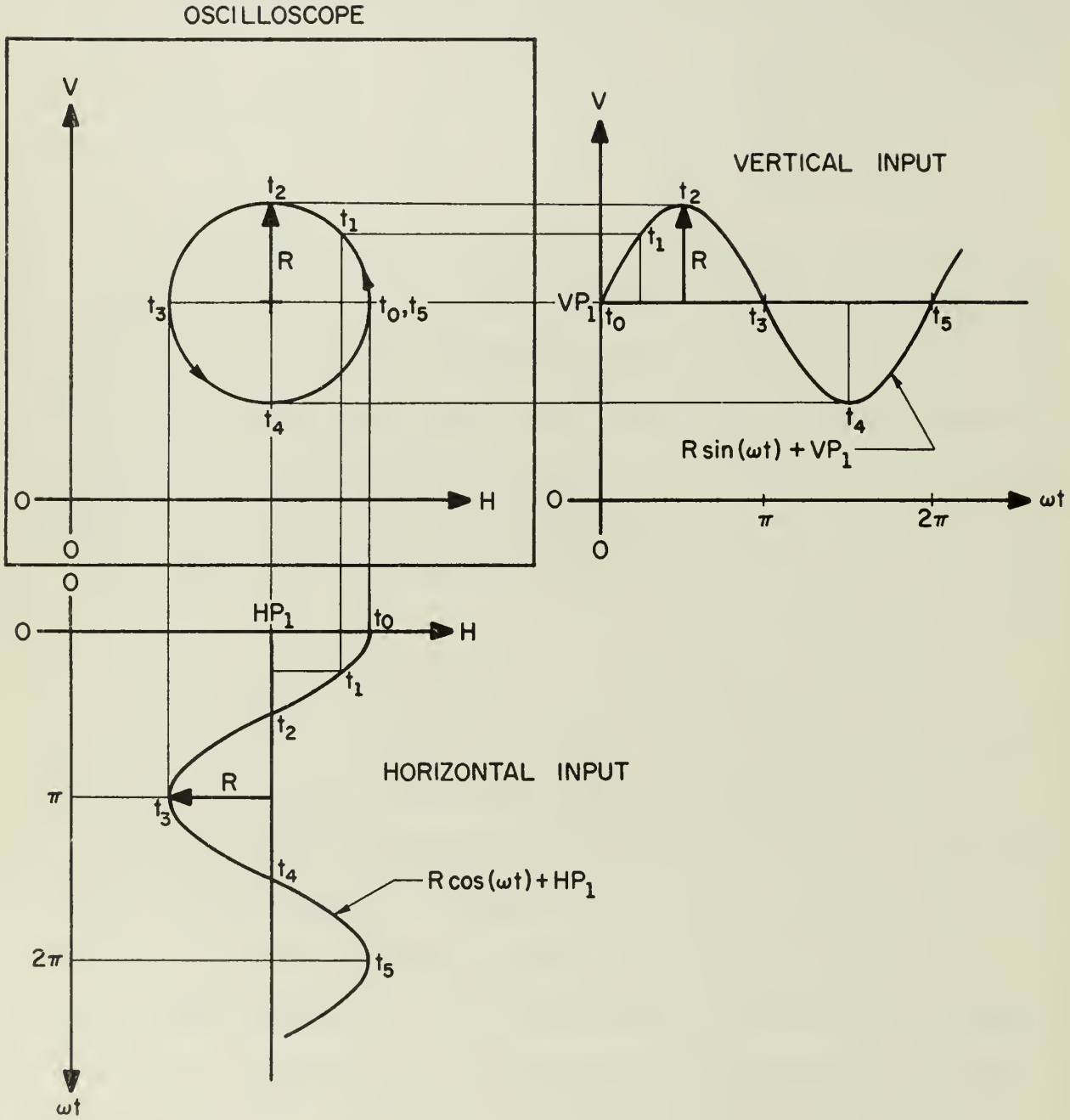

Figure #4. Generation of a Circle with Sine and Cosine Functions.

$-R \sin(\omega t)$ component. And lines of slope other than 45° must have different amplitudes. Another problem that enters at this point is that a line generated by this method extends in two directions from the zero reference. That is to say that a line generated by $+ R_1 \sin(\omega t)$ and $+ R_1 \cos(\omega t)$ will extend from the zero reference (0, 0) to a point (R_1, R_2) and also in the opposite direction to a point $(-R_1, -R_2)$. The first thought to correct this phenomena was to rectify the sinewave, so that only the positive "humps" would reach the deflection plates. This method would work theoretically. However, in practice it was found that one would have to have the negative hump for one type of line and the positive hump for another line, depending on its slope. Also rectification would have to be done not with respect to ground as is usually done, but with respect to some DC offset used to translate the line. These two difficulties, plus the nonlinearities that would create very high-frequency components once the sinewave was rectified, was our reason not to use the rectification approach.

The alternate approach was to add a DC component equal in magnitude to the peak amplitude of the sinewave to the sinewave itself, thereby translating it by exactly the amount it would extend in the undesired direction. This method proved particularly desirable, because digital signals corresponding to the amplitude of the sinewave have to be present, and it was not difficult to generate the corresponding DC offset from the same digital signals. The functions that would now generate a line was of the following form:

$$V = R_1 \sin(\omega t) + R_1$$

$$H = R_2 \sin(\omega t) + R_2$$

where R_1 and R_2 would also be negative if a line of negative slope was desired. It can now be seen that a line generated by the above two functions would extend from the zero reference (0, 0) to $(2R_1, 2R_2)$, and the undesired extension in the opposite direction is eliminated. Consequently by specifying $R_1/2$ and $R_2/2$, one can draw a line from the origin to a second point. This, as in the use of the circle merely corresponds to adding on two DC offsets corresponding to the vertical and horizontal displacement of the first point. The forms of the functions that now describe the generation of a line between any two points (HP_1, VP_1) and $(HP_1 + R_2, VP_1 + R_1)$ is given by

$$V = R_1(\sin(\omega t) + 1)/2 + VP_1$$

$$H = R_2(\sin(\omega t) + 1)/2 + VP_2$$

It should be noted again that R_1 and R_2 can be either positive or negative depending on the slope of the line. Figure #5 shows a graphic illustration of the actual generation of a line.

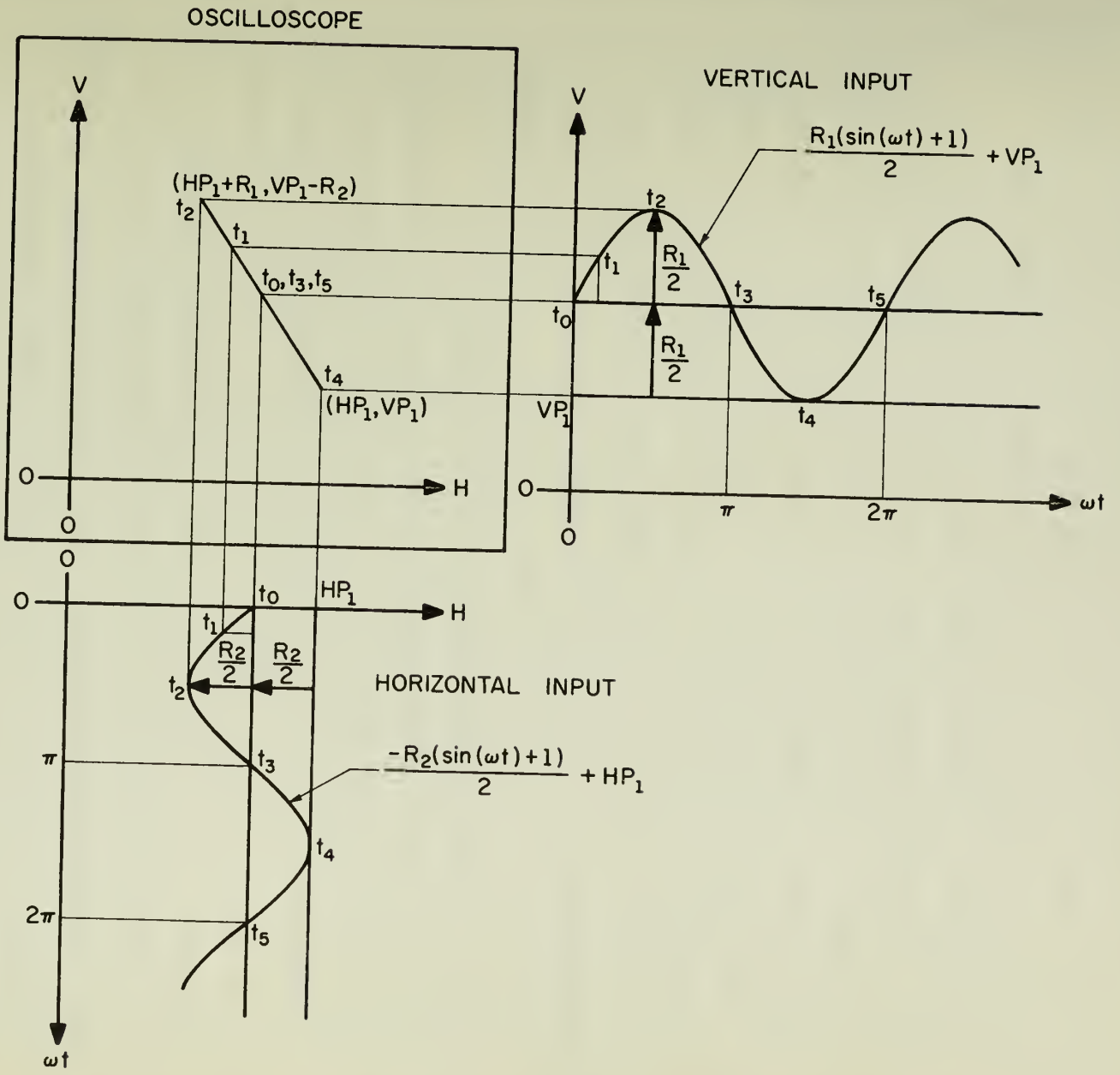

Figure #5. Generation of a Line with a Positive and Negative Sine-function.

4.3 Digital Processor

We can now construct any circle given digital information about the location of its center and the magnitude of its radius. We can also construct any line given the coordinates of the first point of the line and the horizontal and vertical distances to the second point. The problem is how to obtain these digital signals corresponding to the position of points and magnitudes of distances. Since the display used in the Artrix system is of the TV type it was thought to divide the TV raster into a 512 by 512 matrix. In doing so, a "horizontal counter" counted down the 512 points on a horizontal line, and a vertical counter would count down the 512 lines in a frame. Hence the content of the horizontal and vertical counter would contain the digital coordinates of the beam that sweeps out the raster at any time. It should be pointed out that the resetting (or spilling over) of the horizontal and vertical counters are used to provide the horizontal and vertical synchronization signals for the raster that sweeps the TV monitor, the cameras and the storage memories. A 512 by 512 matrix was chosen since this is close to the 525 by 525 resolution that should be found in a "500" line TV system. Furthermore, 512 is the count that can be obtained in a 9 bit counter. If one now controls a second set of counters by the master counters and stops them at some particular time, the count contained in them will correspond to the position of the beam at the time the count was stopped. By detecting the position of the beam with a light sensitive device and using its output to stop the second set of counters one will store in these counters the digital position of the point indicated by the light sensitive device (light-pen). By this method a convenient way of obtaining the

digital position of a point indicated by a light pen has been found. We will call the coordinates of these points horizontal point one (HP_1) and vertical point one (VP_1).

Next, one would like to generate the difference of the coordinates to the second point (clearly those are needed in the equations that describe the lines). This is done by simply starting a third set of counters at the time point one (HP_1, VP_1) was indicated, and stopping them with the second output from the light pen, called point two (HP_2, VP_2). Since the counters spill over and start again from zero once a 511 count has been reached, the magnitude of the count they contain will always be relative to the point one counters and be equal to the difference between point two and point one. An illustration in Figure #6 will clarify this procedure.

As we shall see later the circle operation requires the direct coordinates of point two (not relative to point one). This is done similarly to obtaining point one by using a different gating sequence in starting and stopping the third set of counters.

4.4 Hybrid Processor

We have discussed the production of lines and circles and various digital signals corresponding to coordinates and differences of coordinates on the display. We shall now investigate how these are put together to form lines and circles as indicated on the display. A block diagram of the hybrid processor is shown in Figure #7 and will be helpful in the forthcoming explanations. All control inputs are from the digital processor and are in digital form. All outputs (excepting the one from the

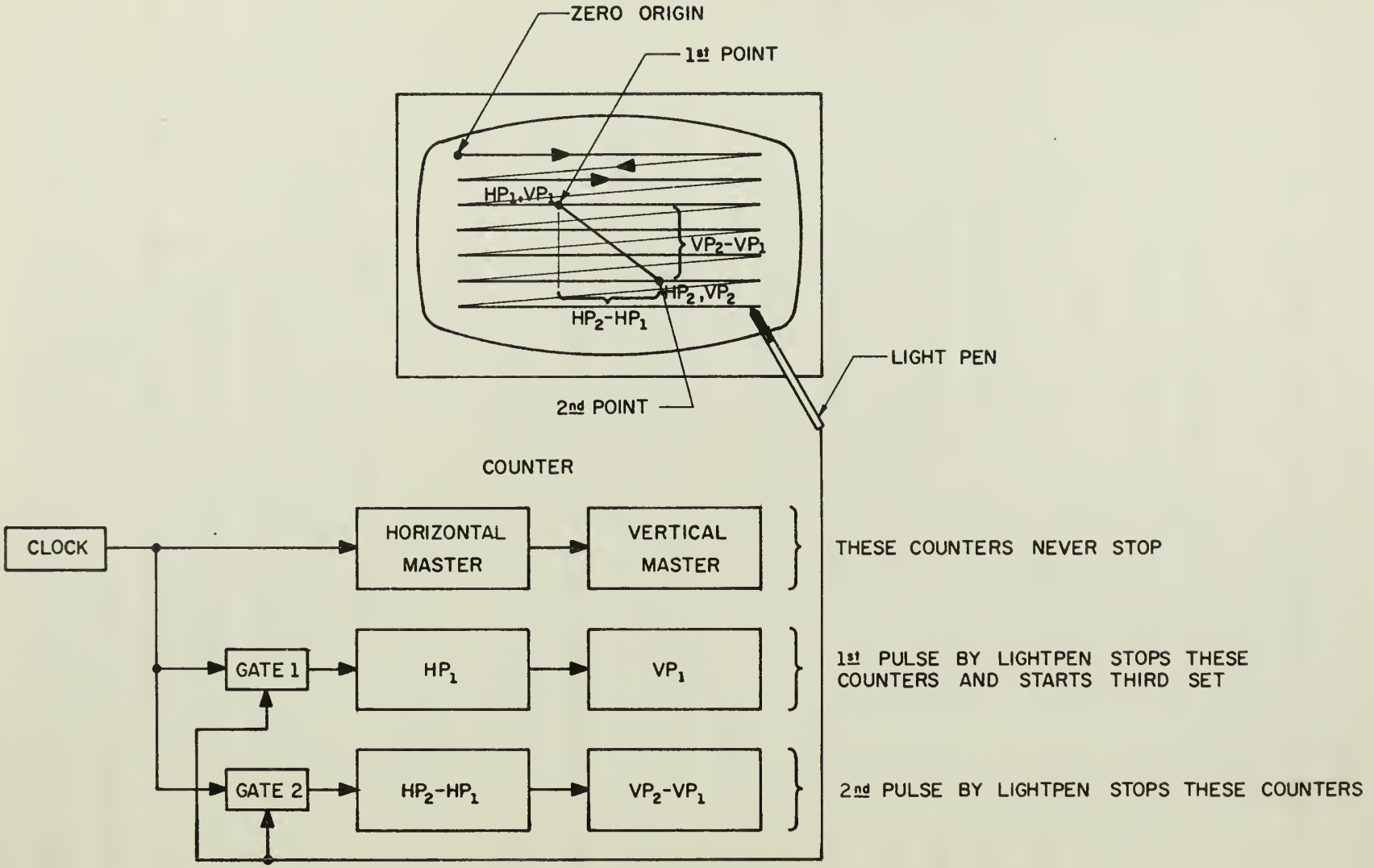

Figure #6. Counter Scheme Used to Obtain Digital Positions of Points.

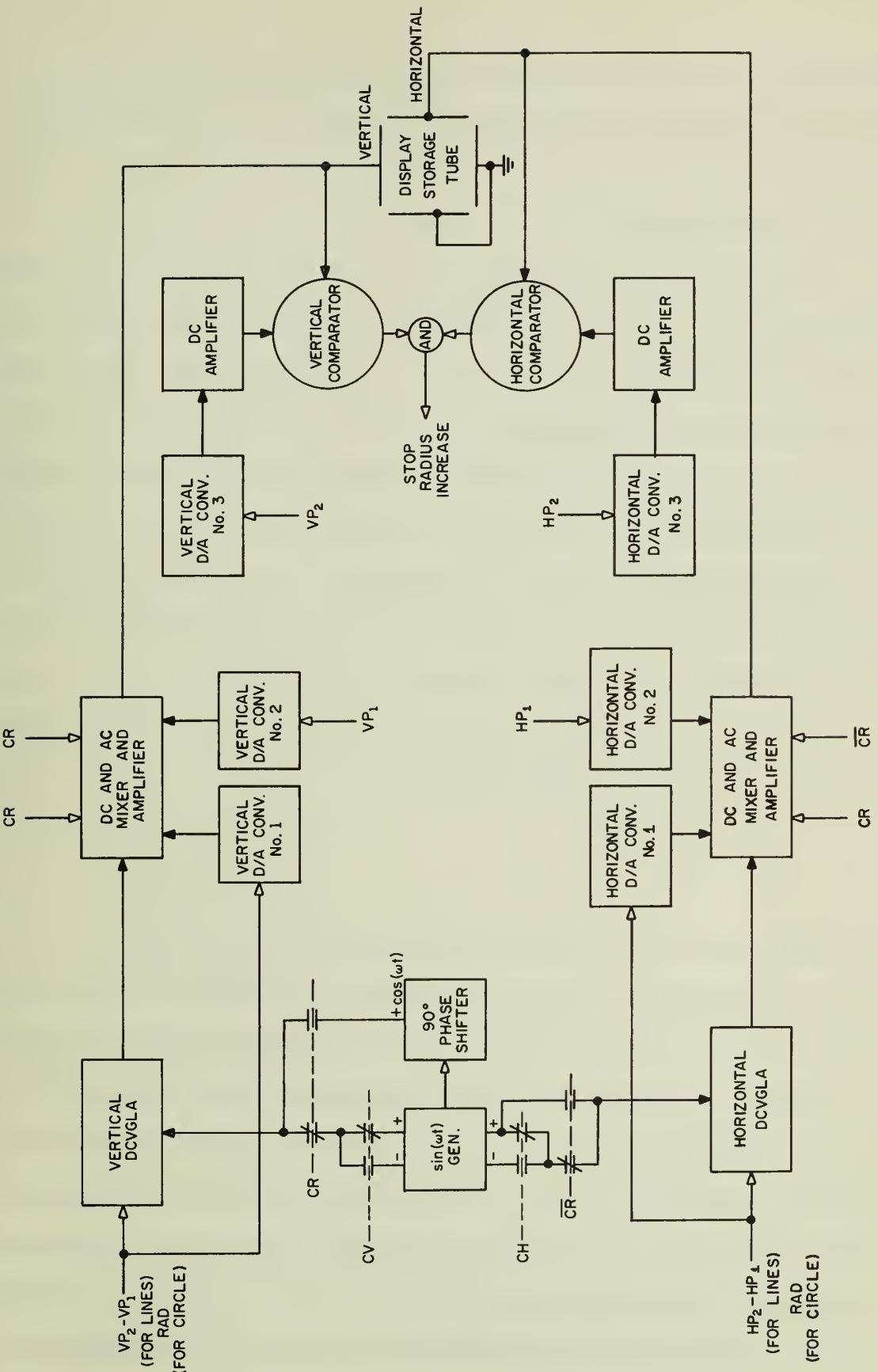

Figure #7. Hybrid Processor.

comparator) are analog, and go directly to the display storage tube. Solid arrows represent analog signals and open arrows represent digital signals.

4.4.1 Circle Operation

Let us consider the operation of constructing a circle. First the processor is switched into the circle construction mode. This selects by means of relays and logic signals CR, CV, CH, a sine and cosine wave. The cosine wave is then applied to the vertical channel and the sinewave is applied to the horizontal channel. The wave manipulations are performed in each channel, except that one uses horizontal digital inputs and the other vertical digital inputs. It should also be noted that the gain of the vertical channel is only 3/4 that of the horizontal channel. This is done to preserve the 3:4 aspect ratio of the TV monitor.

It was shown in Section 4.1 that in order to generate a circle one has to generate the analog signals

$$R \sin(\omega t) + HP_1$$

$$R \cos(\omega t) + VP_1$$

HP_1 and VP_1 are the DC offsets that provide the translations, and are the digital coordinates of the center of the circle. These two digital signals are generated as described in Section 4.3 and are now applied to the digital to analog converters (horizontal and vertical D/A converter #2). The output of these D/A converters are then two DC voltages corresponding to the two DC offsets HP_1 and HP_2. Next the radius of the circle must be found. This is done by a coincidence scheme. The sine and cosine waves are applied to an amplifier whose gain is proportional to a given digital input. (DCVGLA---Digitally Controlled Variable Gain Linear Amplifier).

The digital input to the horizontal and vertical DCVGLA is the same and is stepped from 0 to 511 as long as only the center of the circle has been indicated. The output of the DCVGLA is then a sinusoid that increases with time. This output is then mixed in the DC and AC mixer and amplifier with HP_1 and VP_1 in the horizontal and vertical channel respectively. The vertical and horizontal D/A converters #1 are at this point disabled by CR and $\overline{CR}$. The output of the mixer is then an increasing sinusoid with a DC offset. Next a point on the circumference of the circle is indicated and similarly converted by a D/A converter (#3) to a DC level corresponding to the coordinates of that point. These two DC levels are then compared with the two increasing sinusoids. The desired radius is reached when both sinusoids are equal to the second DC levels (or coordinates of point two) at the same instant. When this coincidence is obtained a logic signal causes the radius counter to stop. In other words: the circle expands about its center until the indicated size (HP_2 and VP_2) has been reached.

4.4.2 Line Operation

Again, as in the circle logic signals CR, CV, and CH select sine or minus sine functions to generate a line. (Actually not all logic signals are available until both endpoints of the line have been indicated since point two determines the slope. This is of no consequence since nothing can be displayed until point two is indicated and settling time of the circuits is much faster than the operator can push the construct button). CR and $\overline{CR}$ signals now enable both #1 and #2 D/A converters that go into the DC and AC Mixer and Amplifier. When point one is indicated, VP_1 and HP_1 are available and are applied to the D/A

converters and fed into the mixer. These then correspond to the coordinates of the first endpoint of the line. Remembering the form of the functions needed for a line from Section 4.2

$$(HP_2-HP_1)(\sin(\omega t)+ 1)/2 + HP_1$$

$$(VP_2-VP_1)(\sin(\omega t)+ 1)/2 + VP_1$$

we see that we must next indicate point two, which gives us (HP_2-HP_1) and (VP_2-VP_1) as shown in Section 4.3.

These are now applied to the DCVGLA to give the sinewave the proper amplitude and to the #1 D/A converters to give the proper DC offset to keep the line from extending through point one. The output of all three signals are then indeed of the form needed to generate the line and are applied to the deflection plates of the display storage tube. No use is made of HP_2 and VP_2 alone in the line mode, and also no comparison methods are needed.

5. HYBRID CIRCUIT DESIGN AND DESCRIPTION

In the following chapter, the hybrid circuits and their design will be discussed. Their implementation and purpose has been described to some extent in Section 4, while this section will deal more with the design considerations.

5.1 DCVGLA (Digitally Controlled Variable Gain Linear Amplifier)

In the hybrid processor need existed for a device that could control the amplitude of a sinewave proportional to a digital input. Specifically a device was needed that would control the amplitude in 512 increments corresponding to 9 digital bits. A mathematical transfer function for this device would be as follows:

$$X = K \sin(\omega t)\left[a_o 2^0 + a_1 2^1 + a_2 2^2 + \ldots + a_8 2^8\right]$$

where $a_o \ldots a_8$ are the binary inputs, K is an arbitrary gain constant and X is the output.

It was decided that the output should have a peak to peak variation from zero to $\pm$ 10 volts in order to maintain compatibility with established voltage levels. A gain constant of $V \approx 1.5$ was found convenient since this would require a 6.67 volt peak sinewave for an input, and this was a convenient value to generate.

The scheme that was used to obtain the above function was one of summing currents through resistors whose values were in the ratio of $2^0 : 2^1 : 2^2 \ldots\ldots : 2^8$, and whose presence in the circuit was determined by a transistorized switch. The scheme is similar to a D/A converter, except that an AC voltage is converted instead of a DC voltage. The AC

must also be able to be changed in phase and in amplitude yet retain the digital control over the signal. A basic diagram of the scheme used is shown in Figure #8, and the actual circuit used is shown in Figure #9. In the actual circuit the constant controlled voltage source was implemented by an emitter follower which used the digital resistance chosen as the emitter resistor. A Darlington configuration for the transistors was chosen to make the source as "stiff" as possible. This would give the circuit a current gain of about $\beta_1 \cdot \beta_2$ where β_1 and β_2 are the respective betas of the 2N2102 and 2N3054. This proved to be adequate for the change in the emitter resistor from R/2 to AC open circuit. A DC bias current had to be present to keep the transistors in the active region. An 8 Hy coil was put in series with the bias resistor to make it look like an AC open circuit at 10 KHz.

Current sensing is done in the collector of the Darlington pair. A transformer was chosen as the current detection device. It provides complete DC isolation from the rest of the circuit, it gives great voltage gain, and provides the needed impedence match. The AC resistance in the collector should be small compared to the minimum AC resistance found in the emitter. The load on the secondary of the transformer is 10K. Its turns ratio is such as to present 3 ohms in the primary: 3 ohms in the collector is small compared to a minimum of 100Ω in the emitter. Using this value as a standard, the R_o in the digital emitter chain was chosen close to 200 ohms. Since it is difficult to get precision resistors such that the R_o is 200Ω $\pm$ .1%, and since the saturation resistance of the transistor switch would add an even greater error, it was decided to use adjustable resistors in the first six most

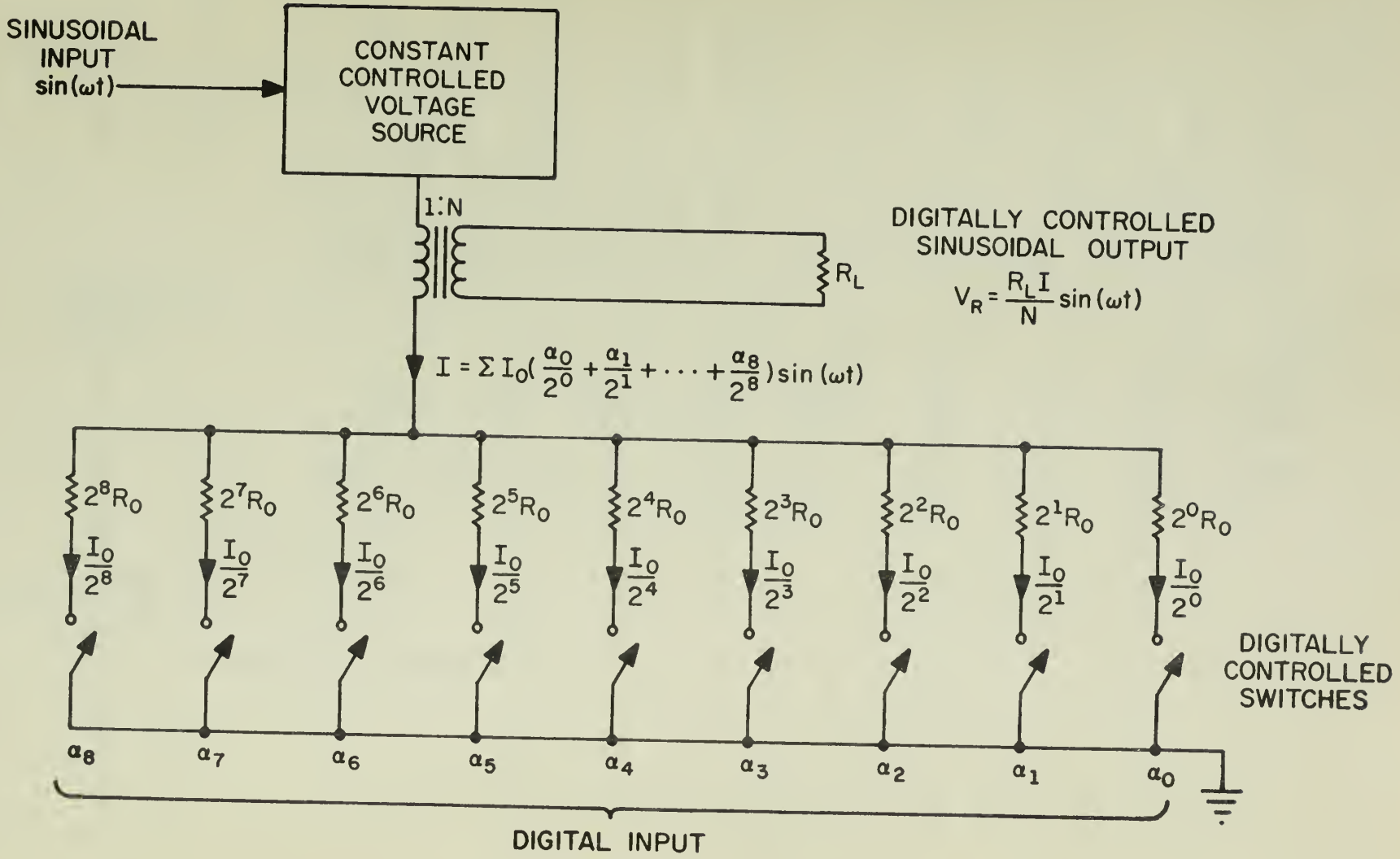

Figure #8. Basic Scheme of DCVGLA.

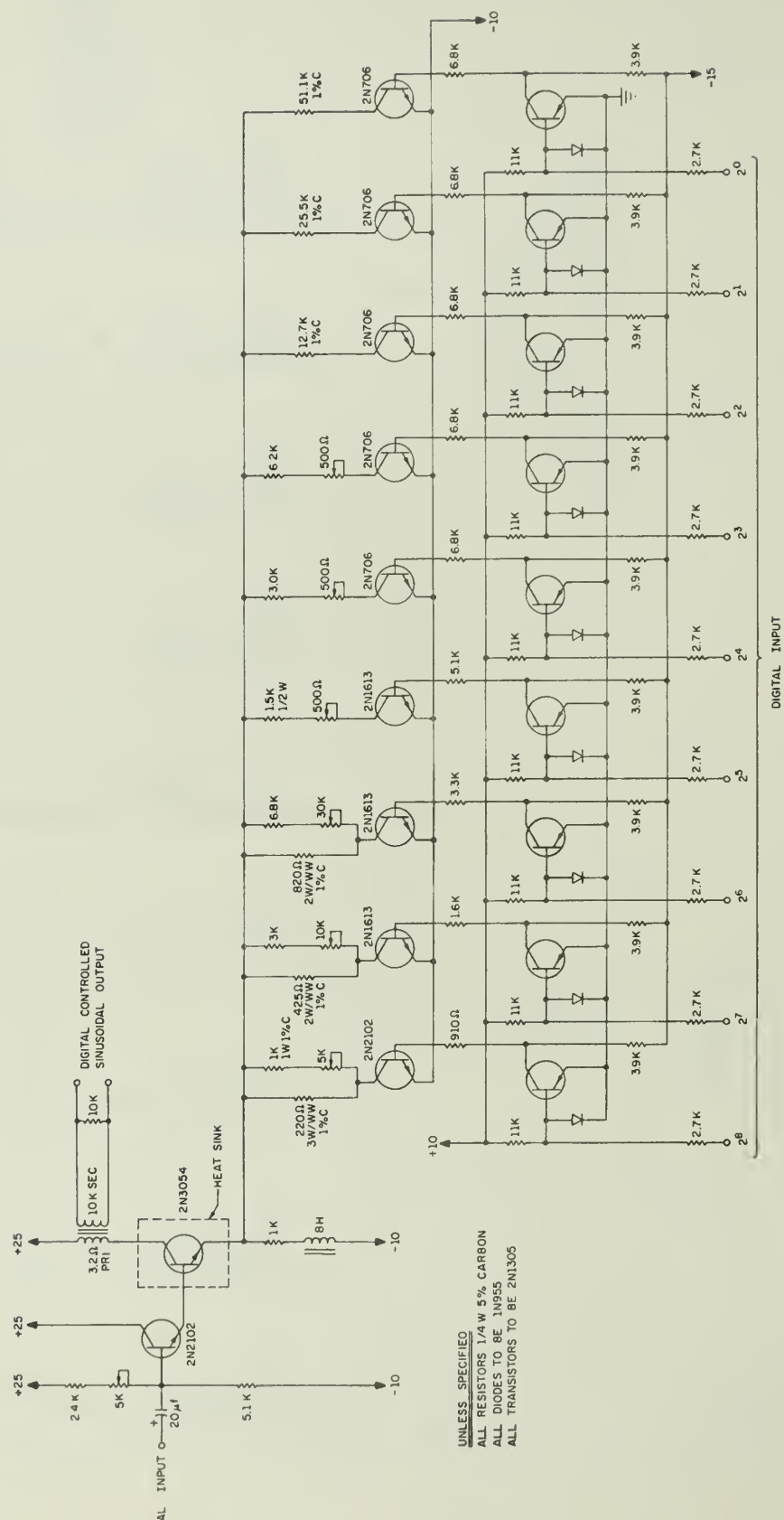

Figure #9. Schematic Diagram of DCVGIA.

significant bits of the chain. For the last three bits 1% resistors were found adequate, and at this value ($2^6 R_0$) the saturation resistance of the transistor was also negligible. The resistance chain was adjusted such that any two adjacent bits would provide an output voltage in the ratio of 2:1. The switching in and out of the resistor was accomplished by a two stage switching circuit. Two stages were needed to provide compatibility with the logic levels of the digital system, and to provide the high gain needed to drive the first two most significant bits. Peak currents of the order of 200 ma are expected to flow through the transistor turning the most sifnificant bit on and off. The accuracy of the system is one part in 512 or about .2%. The limiting factor in adding on more bits is that the resistance of the least significant bit be less than the total parallel resistance of the backbiased collectors of all the other legs. Another way of looking at this is to note that the current flowing in the least significant leg be greater than the total leakage currents in all the other legs. The other limiting factor is that the AC open path in the bias drive indeed look large compared to the resistance of the least significant bit.

It was this factor that limited the accuracy of the circuit. We used an inductance of 8 Hy to provide an AC impedance of about 500K compared to about 50K in the path of the least significant bit.

5.2 D/A Converter

The D/A converter is essentially a much simplified version of the DCVGLA. There are several things that simplify its design consideration. For one thing, we are only concerned with DC levels: There are no AC components. This eliminates bias problems and AC isolation immed-

iately. The detection mechanism can now be a differential amplifier sensing current through a resistor. The need for a constant controlled AC source is eliminated, since the DC supplies can essentially perform this function. The need for high power levels, and hence a two stage switch is also eliminated, because there is no AC open circuit bias chain that puts a limit on the resistance of the least significant bit. The limiting factor is now the leakage current in the rest of the chain, which can be made extremely small, by choosing low leakage transistors. A basic diagram of the D/A converter is shown in Figure #10 and Figure #11 shows the actual circuit configuration. Conversion accuracy of the circuit is one part in 512, and maximum conversion frequency was about 2.5 megabits per second. That is to say that any bit can be switched at a 2.5 MHz rate and the output will produce a 2.5 MHz waveform. The limitation of the uppermost conversion rate is governed by the RC time constant of the least significant bit. The value of the summing resistor R should be small compared to the resistance R_o in the most significant bit of the binary resistance chain. The output variation for a zero to 511 digital input variation was -10 volts for zero and -14 volts for 511. These levels had to be amplified again in the mixer stages in order to be compatible with the $\pm$ 10 volt swings required for full screen deflection. Zero volts horizontal and vertical would represent the center of the screen. Performance of the D/A converters proved excellent throughout the use in the system.

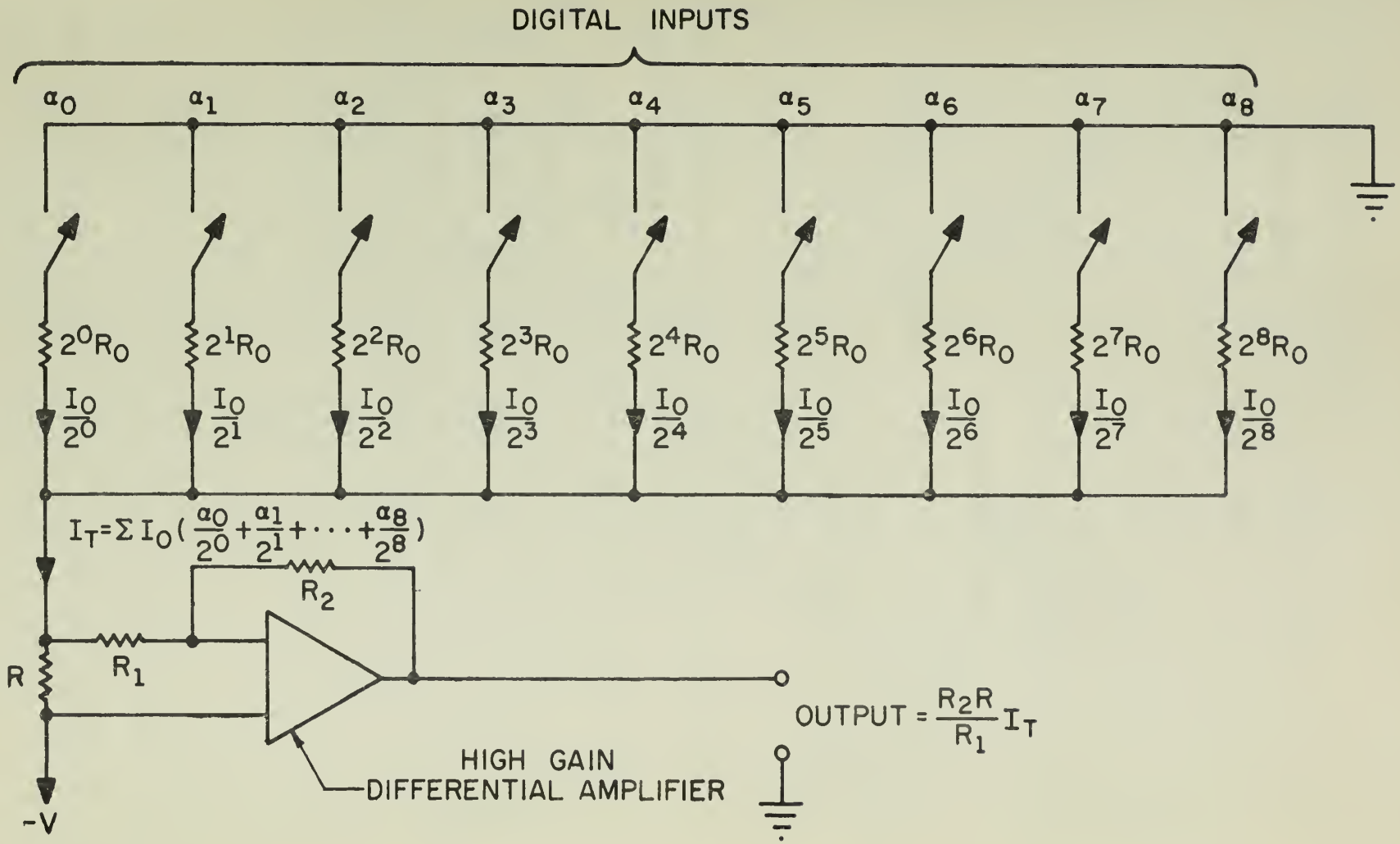

Figure #10. Basic Scheme of D/A Converter.

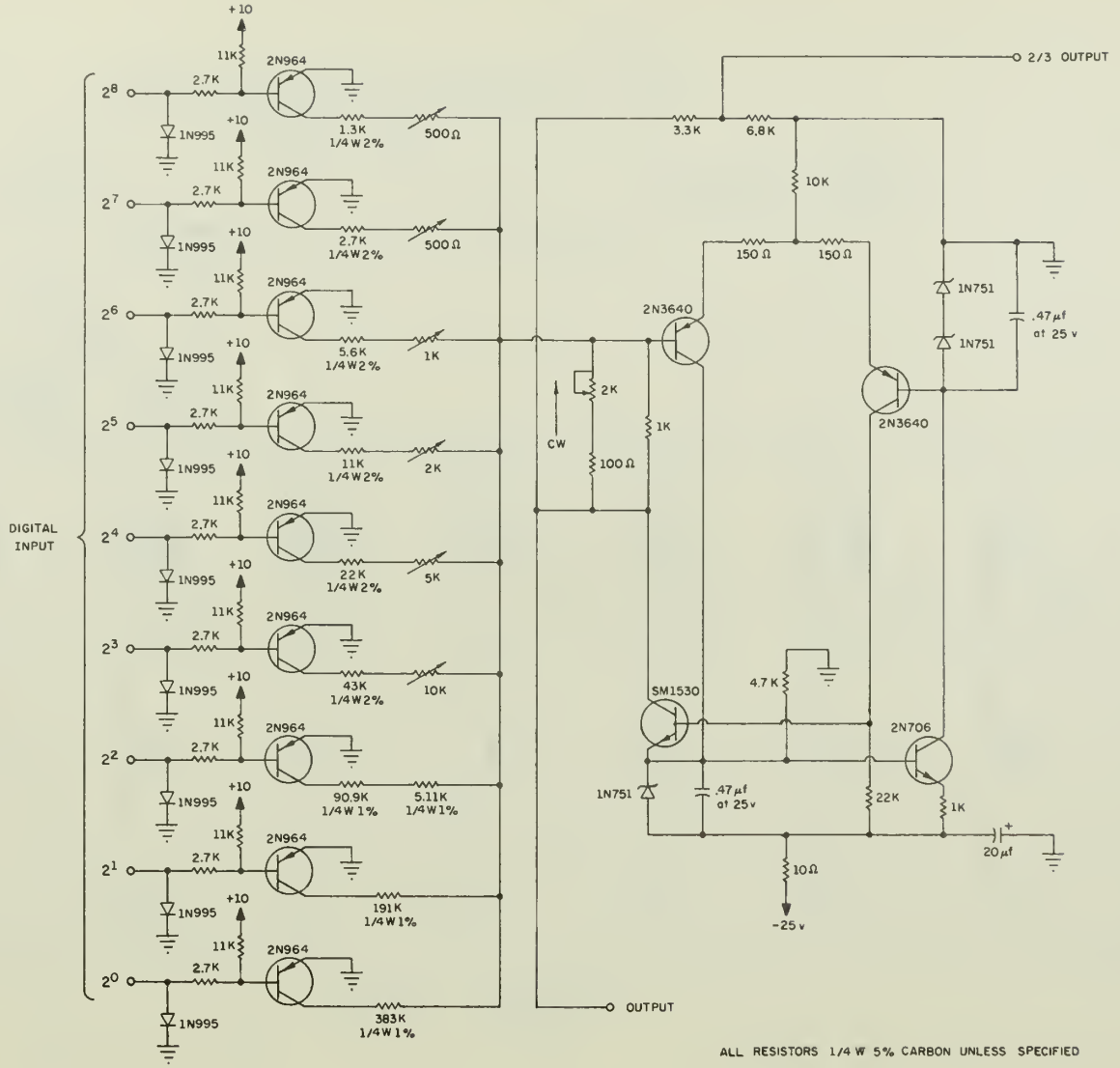

Figure #11. Schematic Diagram of D/A Converter.

5.3 DC and AC Mixer and Amplifier

Another analog circuit with digital control is the DC and AC mixer and amplifier. It was designed to perform several functions, two of which depend on the presence or absence of a digital signal. The operations the circuit can perform are the following. First, the circuit is a precision adding or subtracting circuit of DC levels. Second, it is a compensated differential DC amplifier. Third, it is a mixer which takes the DC level (DC offset) of a D/A converter and mixes it with one of the sinusoids. As mentioned above it can be digitally controlled to perform addition of two variable levels, or addition of one variable and one fixed level. The circuit is also an output buffer for the hybrid processor. Figure #12 gives a complete schematic of the circuit. Operation of the circuit is as follows.

First let us consider the digitally controlled DC adder and subtractor. The digital control signal corresponds to either line or circle operation. For the line operation (Section 4.2) a DC offset of the same magnitude as the sinusoid is added in to prevent extension of the line through point one. Also, another DC offset was needed that would translate point one to the proper point on the screen. The digital signal for line operation selects current source I_2 in this mode. Both current source I_1 and I_2 are controlled sources. I_1 is controlled by the D/A converter that determines translation, and I_2 is controlled by the D/A converter that determines the additional DC offset to prevent extension of the line through point one. These two currents are then summed through R_s and the voltage across

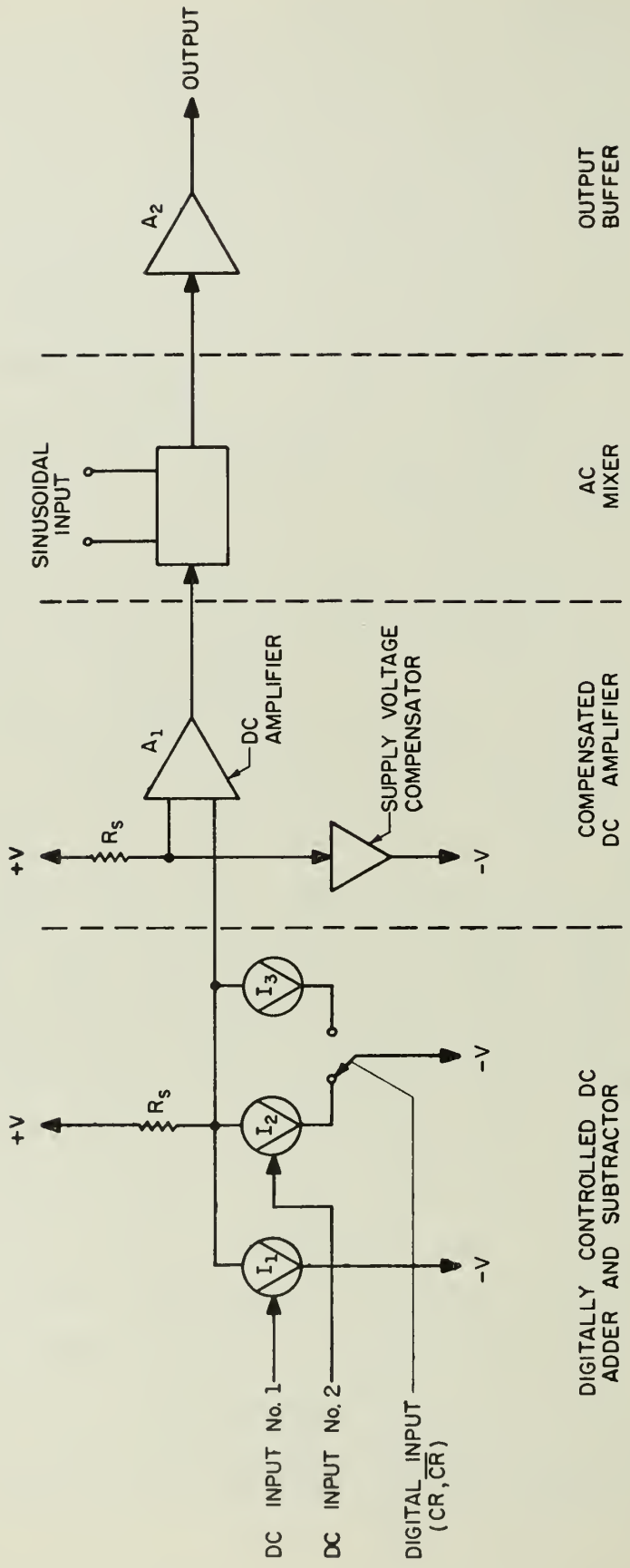

Figure #12. Basic Scheme of DC and AC Mixer and Amplifier.

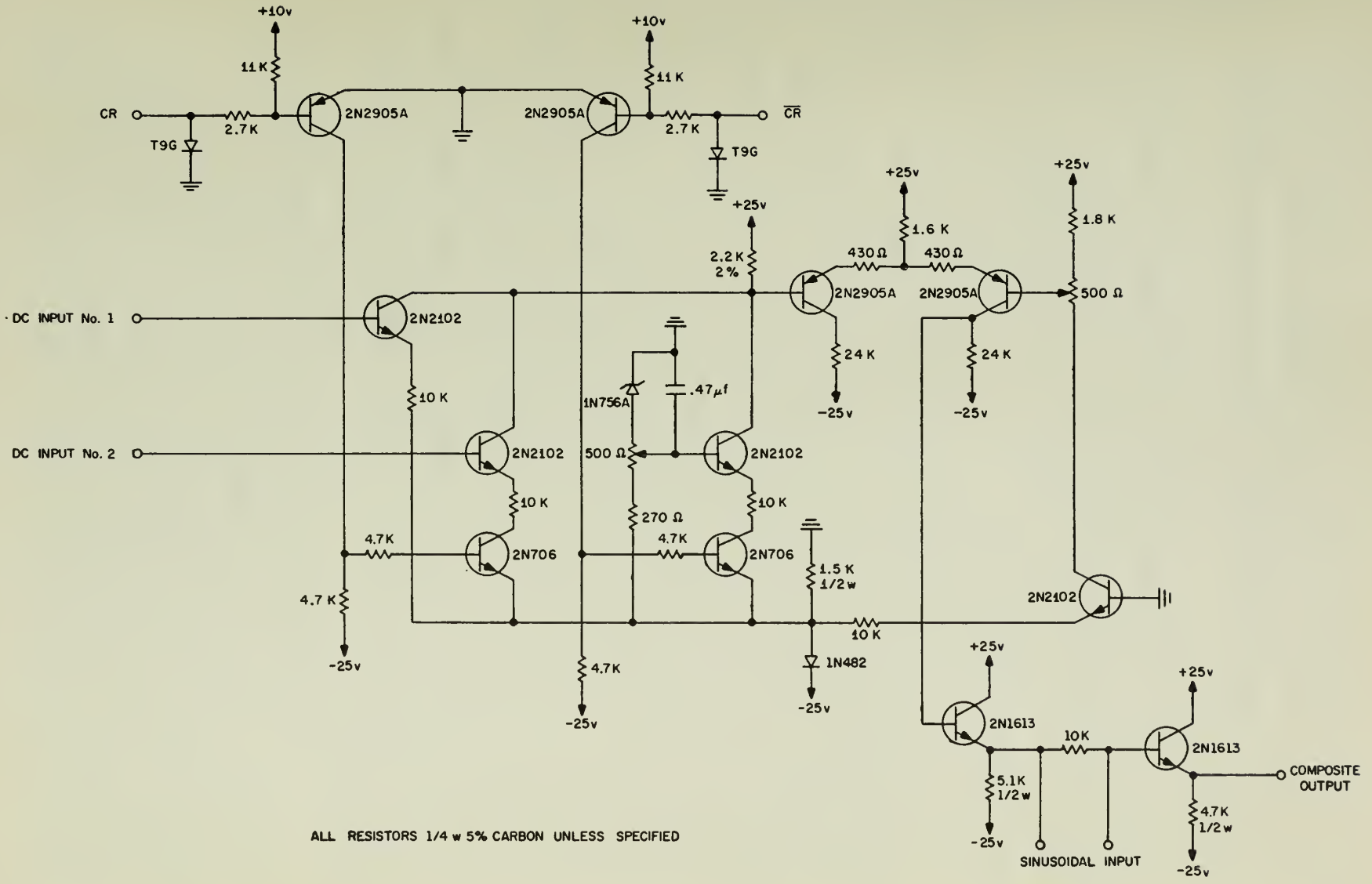

Figure #13. Schematic Diagram of DC and AC Mixer and Amplifier.

R_s is proportional to the sum of the currents. If one of the currents is negative with respect to a new reference, subtraction will take place.

When the system is in the circle operation, the additional DC offset due to source I_2 is not wanted. The digital control then selects I_3, which is a fixed current source that is equal to the zero reference mentioned above. Since it is at zero reference it does not add on any translation to the center of the circle. It is, however, necessary, since zero reference differs from ground or zero current at this point. This fixed current reference can be adjusted by means of a potentiometer to the correct value. The controlled current sources are essentially emitter followers, whose collector currents are summed through a 2.2K resistor (R_s). The output of the adder is then applied to a compensated DC amplifier whose gain is such that a $\pm$ 10 volt variation occurs at its output. The compensation circuit was designed to prevent drift due to supply variations. The reference to the differential amplifier is essentially of the same configuration as the DC equivalent of the signal source. Hence through common mode rejection the supply variations are eliminated at the output.

The other function is the mixing of the sinusoids with the DC levels. This is done by applying the DC to our emitter follower, and putting in series with the output the output transformer of the DCVGLA. The AC is developed by the DCVGLA across the 10 K resistor and added on to the DC present on the emitter resistor of the emitter follower. The output of this series circuit is then tied to another

emitter follower, which serves as a high input impedance to the mixer and a low output impedance to the rest of the system. This is the output buffer mentioned before. The performance of the circuit in the system proved excellent. Variations in switching from one mode of operation to another were not noticeable by eye on the display screen. Temperature and voltage stability proved excellent compared to an uncompensated previous circuit.

5.4 Plus and Minus Sine and Cosine Generator

In order to generate the lines and circles for the processor it was necessary to provide the ± sine and cosine functions. These had to be extremely linear and practically void of all higher harmonics. The phase relationship between the functions had to be controllable and fixed to within onehalf of one degree: Otherwise circles would appear elliptical and lines would look like an extremely long or narrow ellipse. Phaseshift had to be controllable to compensate for phaseshift in the amplifiers of the rest of the system. Any higher harmonic distortion would cause circles to have bumps in them and lines would exhibit figures that resembled a profile of a twisted pair of lines. It turns out that Lissajous patterns are an excellent measure of linearity for sinusoidal waveforms, so in checking linearities the desired end product was used as a measuring tool.

The entire circuit consists of four sections. First a sinusoidal oscillator, second an amplifier, third a phaseshifting network, and fourth, an output buffer network with amplitude control of each sinusoid. A schematic diagram of the circuit is given in Figure #14.

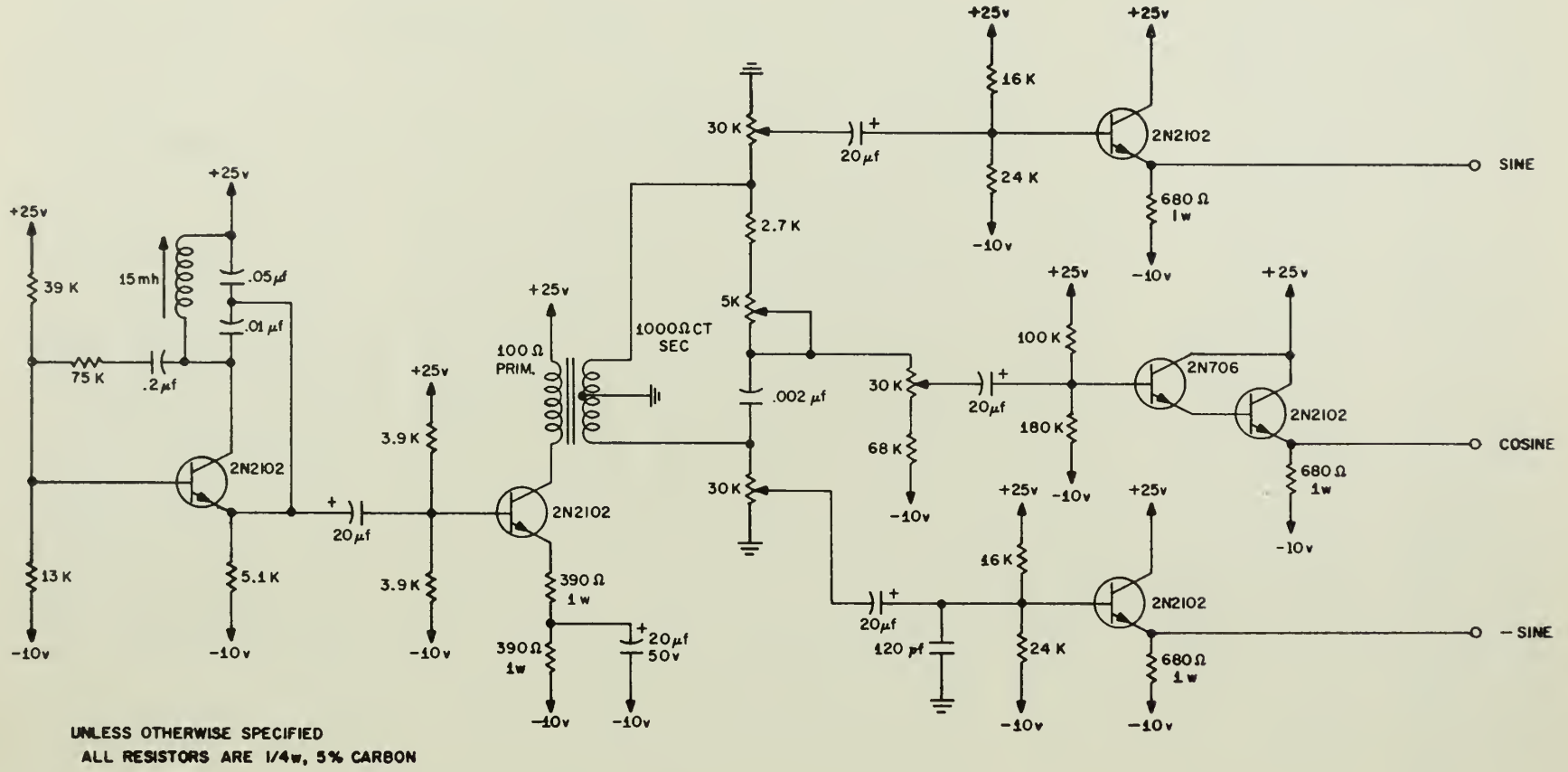

Figure #14. Schematic of Plus and Minus Sine and Cosine Generator.

For the oscillator a Colpitts configuration with emitter feedback was used. Since frequency stability is of no consequence a freerunning LC tuned configuration proved adequate. To get the greatest linearity the loop-gain was adjusted such that it is as close as possible to one. A frequency of 10KHz was chosen so that the response time of the comparator would not be exceeded. Also at this frequency any third harmonic distortion, which was prevalent, did not pass through the transformer used in the phaseshifting network and the DCVGLA. The amplifier used was a simple single ended class A configuration with transformer output. The only caution that had to be observed was not to saturate the transformer. This transformer also served as the heart of the phaseshifting network. By grounding the center of the transformer, the two ends of the winding have two signals that are 180 degrees apart. These provided the $\pm$ functions. By taking a resistor R and a capacitor C whose reactance at 10KHz is equal in magnitude to R one can obtain a signal exactly 90 degrees out of phase with either end of the transformer by applying this series combination of R and C across the transformer. This signal was then the cosine function. By making R variable the phase of the consine function could be adjusted separately. The outputs of the transformer and phaseshift networks are controlled by potentiometers and fed to emitter followers to provide a buffer for the next stage. A Darlington configuration was used for the cosine function since its phase stability was more dependent on the input-impedance into the emitter follower. The circuit exhibits excellent linearity at this point and perfect lines and circles can be obtained.

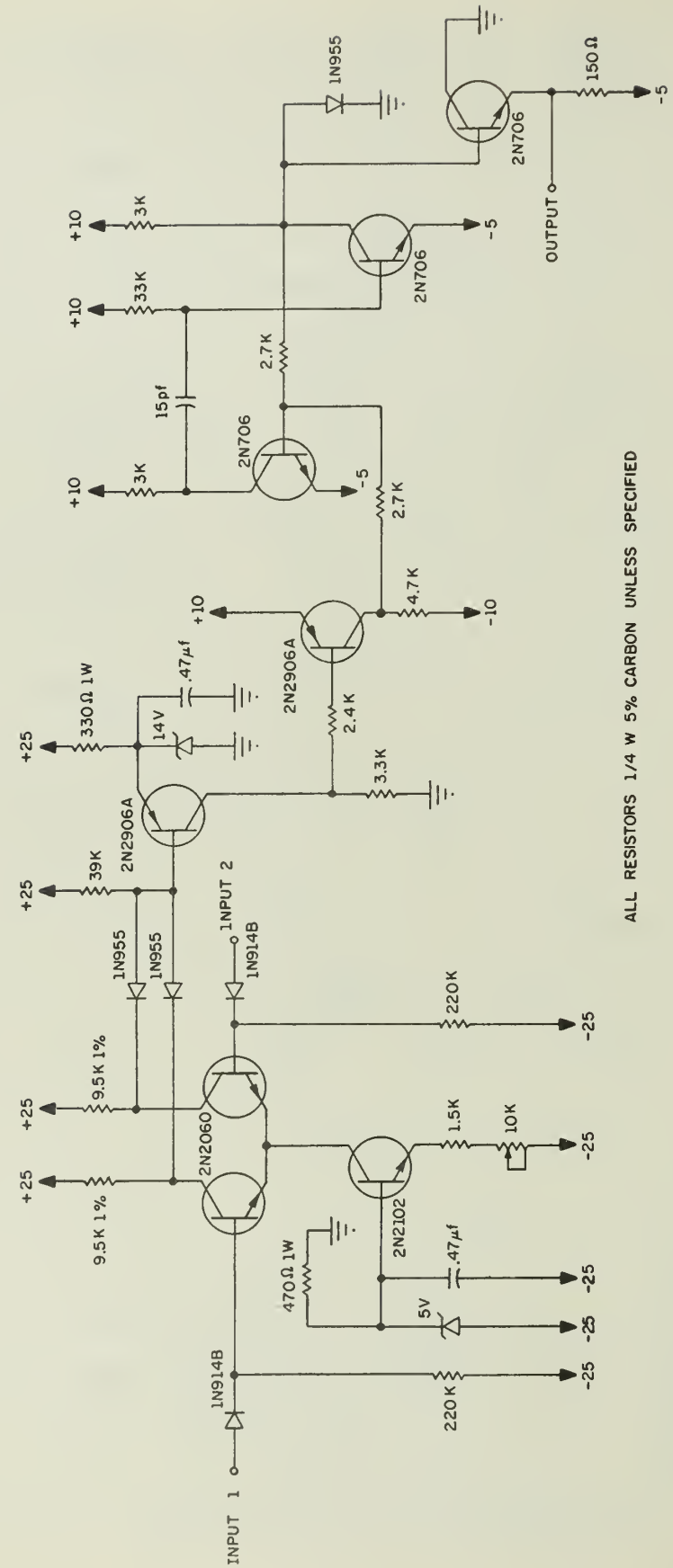

Figure #15. Schematic of Comparator.

5.5 Comparator.

It was explained in Section 4.1 that radii of circles were determined by a comparison method. The expanding sinusoids were compared to the DC levels of the horizontal and vertical portions of point two. Upon coincidence of both vertical and horizontal voltages the radius was stopped from increasing.

The circuit configuration is shown in Figure #15. It consists essentially of three sections. First the differential amplifier, second a "NOR" circuit to sense two equal voltage levels, and third a single-shot to provide an output pulse of fixed width.

In considering the differential amplifier, one must realize that it must be able to compare any two voltages in the range of ± 10 volts. Since it is conceivable that one input can be + 10 volts while the other might be -10 volts, a differential voltage of this magnitude will break down the base to emitter junction of most transistors, so special precautions must be taken. A diode with a high breakdown voltage must be used in series with the base. The diode is forward biased by a 100K resistor tied to -25 volts. A constant current source is used in the emitter circuit of the differential amplifier to provide high sensitivity. When both inputs are equal, current splits evenly between the two legs of the amplifier, and the "NOR" circuit is such that it changes state when the voltage in both legs of the circuit are equal. This change indicating equivalence is used to trigger a single shot of .2μs duration. Since accuracy of 1 part in 512 is desired the period of the 10KHz was divided by 512 to arrive at the .2μs duration.

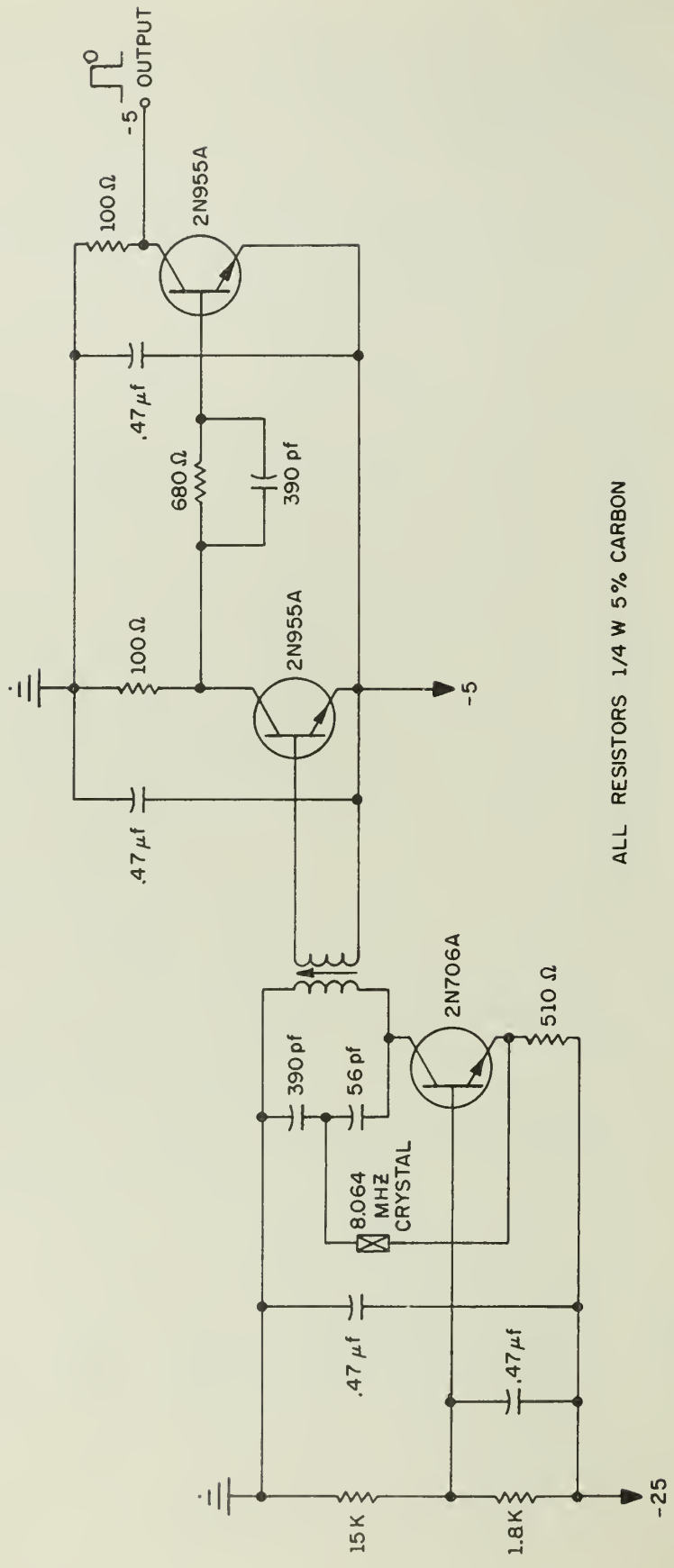

Figure #16. Schematic of 8,064 MHz Clock.

The circuit will respond to a differential offset of 30 mv. This falls within the desired sensitivity of 40 mv. (This was obtained by dividing the maximum voltage variation by 512 which is the quantized voltage change). It was found that the sensitivity of the comparator could be maximized by adjusting the value of the current source. This would essentially set the threshold for the "NOR" circuit. Performance of the circuit showed good results in as far as radii of circles could be determined accurately and consistently.

5.6 8,064 MHz Clock

In order to divide a horizontal line of 62.5 μs duration into 512 points a fundamental clock frequency of 8,064 MHz was needed. This clock would provide the synchronization signals for the entire system. To get the best stability and frequency accuracy a crystal controlled circuit was designed. A schematic of the circuit is given in Figure #16. The configuration is a crystal controlled Colpitts circuit with tuned collector and emitter feedback with the crystal. The circuit is driven hard to provide good stability. Since a square wave is needed to drive the logic circuits of the processor, two transistors are used in a squaring circuit. The tuned collector has a secondary winding which feeds directly into the base of the first transistor. This transistor in turn drives the output transistor of the circuit. The output is a square wave with rise and fall transitions of less than 20 ns. At these speeds decoupling of the supplies through the closest physical path is of primary importance in maintaining a clean waveform with fast rise-time. Without this precaution severe overshoot and ringing took place. Layout of the circuit on

the printed circuit card was done in such a way as to obtain short interconnections.

5.7 DC Adder and Amplifier

This circuit is basically similar to the one shown in Section 5.3, but with some simplifications. It only amplifies DC and mixes it with the sinusoids, rather than mixing two DC voltages together also. The circuit configuration is shown in Figure #17. The first section takes the DC voltage of the D/A converters and amplifies it by a factor of four. This is done with a differential amplifier whose second input is the zero reference of the D/A converters. It can be adjusted by a potentiometer in the emitter circuit. This merely allows one to change the effective zero reference of the D/A converter input. The next section is an emitter-follower and level changer. The level is changed such that the DC output is centered with respect to ground. It is also used to provide a source for the mixer. Mixing is done in the same way as in the circuit of Section 5.3. That is, the transformer output of the DCVCLA is put in series with the emitter follower of the previous section, and then fed into another emitter follower. This last stage provides an output-buffer to the rest of the system. Through use of a differential amplifier, good stability is obtained. Also a low gain factor makes the circuit insensitive to drift.

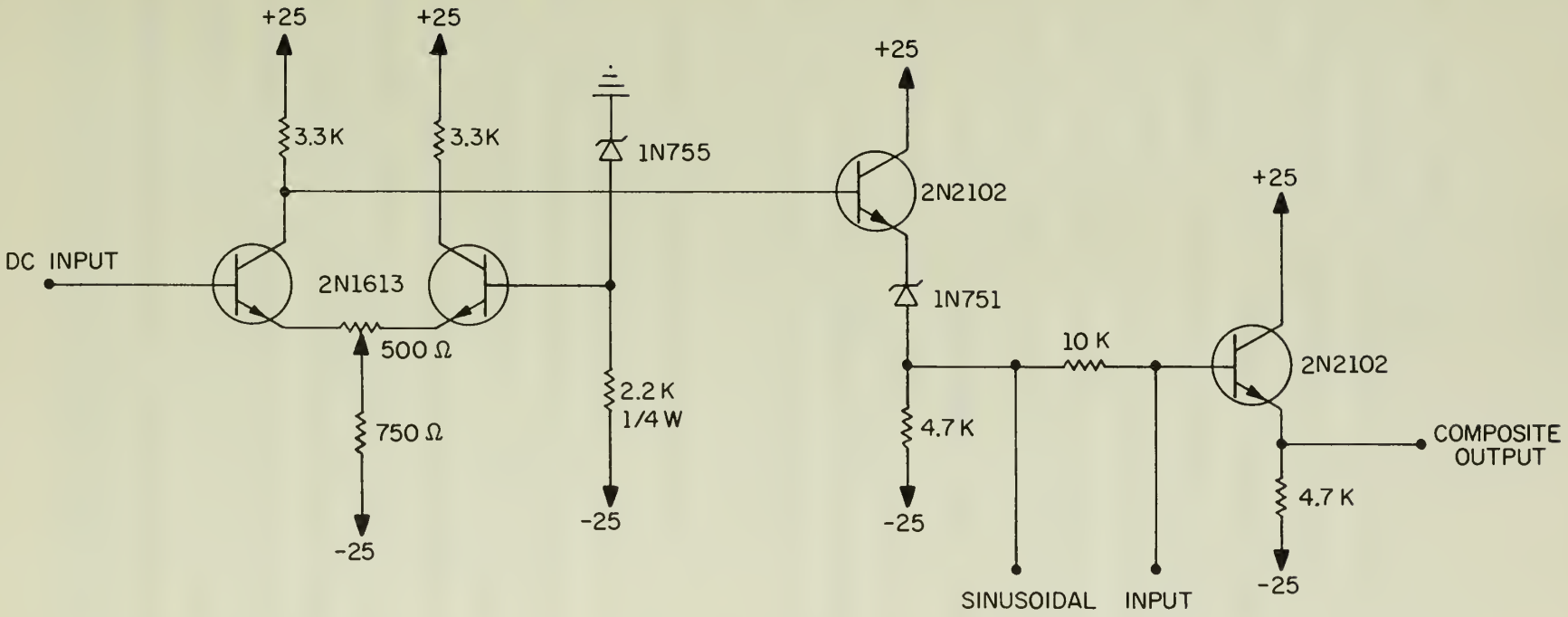

Figure #17. DC Adder and Amplifier.

6. CONCLUSION

It can now be seen that through the effective use of hybrid digital-analog circuitry, (on which the most effective use of the desirable properties of each technique is made), one can perform all euclidian constructions without the use of a large scale digital computer.

The digital processor of the graphical display, and its associated counters divide the screen into 512 x 512 points and provides a digital output for indicated positions or distances. Obviously a digital counter can perform these functions very well. To generate the lines and circles in a trivial manner analog circuitry is used to form Lissajous patterns. To use digital techniques at this point would require a great deal of computational equipment. Analog circuitry is the only simple way out. Now the analog information must be combined with the digital information. This is done with the newly developed hybrid circuitry. It digitally controls the amplitude phase as well as the routing of the analog signals. It is this close merging technique which allows one to perform seemingly complex operations in a simple manner. The speed of the system is also very high, since the display of constructions is done by a continuous analog wave form rather than a point by point plotting routine. Once the shape of the waveform has been determined by a set of counters and a digital-analog interface, no more calculations have to be done to continuously display a construction. Again one can see that the advantageous points of each system are used and then merged together.

Unfortunately, one also inherits some of the disadvantages of each system in this type of operation. These difficulties, however,

are not insurmountable, and usually just represent an upper limit to speed and precision. Analog information is limited in accuracy since it is hard to differentiate between two nearly equivalent voltages (or currents) over a large range. For a 512 by 512 point system this was no problem, but for a 1000 x 1000 point system the problems of accuracy would become more severe. A digital system is usually more accurate in the sense that even a very small digit is still represented by a "0" or "1" condition which is readily recognized. The disadvantage of a digital system however is that one would need as much circuitry as one wants accuracy in digits. For instance, one can store an analog number on a capacitor, and if the detection circuit is accurate, one can resolve this level to a certain accuracy. To store this voltage by digital means to the same accuracy would obviously require more than a capacitor and a detection circuit. Again these difficulties can be overcome by more elaboration in the involved circuitry.

Another problem that was noted in the design of the Artrix system was that of drift caused by aging, temperature variation, etc. Great care should be taken to have all analog signals as stable as possible. In most cases drift tends to be a cumulative rather than a canceling effect, and when an accuracy of one point in five hundred has to be maintained, this can become significant. Again, the high resolution is somewhat limited by the drift that might occur due to temperature variations and elaborate precautions should be taken for higher resolution systems.

Despite these minor difficulties hybrid processing offers many advantages and shortcuts over present all-digital or all-analog

systems. It is felt that hybrid systems are very worthwhile and should be used wherever high speed, simplicity, and limited accuracy are called for.

BIBLIOGRAPHY

"Quarterly Technical Progress Report", (Hardware Systems Research), Department of Computer Science, University of Illinois, Urbana, Illinois. July-September, 1965.

"Quarterly Technical Progress Report", (Hardware Systems Research), Department of Computer Science, University of Illinois, Urbana, Illinois. October-December, 1965.

"Quarterly Technical Progress Report", (Hardware Systems Research), Department of Computer Science, University of Illinois, Urbana, Illinois. January-March, 1966.

"Quarterly Technical Progress Report", (Hardware Systems Research), Department of Computer Science, University of Illinois, Urbana, Illinois. April-June, 1966.

Pulse, Digital, and Switching Waveforms, Millman, Jacob, and Taub, Herbert. McGraw-Hill Book Company, 1965.

Selected Semiconductor Circuits Handbook, Schwartz, Seymour, Editor. John Wiley and Sons, Inc. 1960.